

WHAT IS CLAIMED IS:

- 1        1.     A transceiver, comprising:
  - 2              a first interface configured to receive data from a first channel using a first
  - 3              clock signal and to transmit data to the first channel using a second clock signal;
  - 4              a second interface configured to receive data from a second channel using a
  - 5              third clock signal and to transmit data to the second channel using a fourth clock
  - 6              signal; and
- 7              a re-timer configured to re-time data received from the first channel using the
- 8              first clock signal and to retransmit the data to the second channel using the fourth
- 9              clock signal.
- 1        2.     The transceiver of claim 1, wherein
  - 2              the first channel includes a first clock line for transmission of the first clock
  - 3              signal and a second clock line for transmission of the second clock signal and the
  - 4              second channel includes a third clock line for transmission of the third clock signal
  - 5              and a fourth clock line for transmission of the fourth clocks signal;
  - 6              the transceiver further comprises:
    - 7              a first receiver configured to receive data and the first clock signal from the
    - 8              first channel;
    - 9              a first transmitter configured to transmit data and the second clock signal to
    - 10             the first channel;
    - 11             a second receiver configured to receive data and the third clock signal from the
    - 12             second channel;
    - 13             a second transmitter configured to transmit data and the fourth clock signal to
    - 14             the second channel; and
    - 15             the re-timer is located between the first receiver and the second transmitter and
    - 16             is configured to re-time data received from the second channel using the third clock
    - 17             signal for retransmission, using the second clock signal, onto the first channel.
  - 1        3.     The transceiver of claim 1, wherein data received by the first interface from
  - 2              the first channel using the first clock signal is first data; and the transceiver further
  - 3              comprises isolation logic to prevent the transceiver from transmitting the first data
  - 4              from the first interface to the first channel using the second clock signal.

- 1       4.     The transceiver of claim 1, further comprising isolation logic to prevent  
2     retransmission of data, received from the first channel, to the second channel.
- 1       5.     The transceiver of claim 1, further comprising latch-up prevention logic to  
2     prevent feedback of data between the first and second channels.
- 1       6.     The transceiver of claim 1, further comprising a first synchronizing unit that  
2     synchronizes data transmitted from the first channel to the second channel.
- 1       7.     The transceiver of claim 6, further comprising a second synchronizing unit that  
2     synchronizes data transmitted from the second channel to the first channel.
- 1       8.     The transceiver of claim 1, wherein the third and fourth clock signals are  
2     synchronized to the second clock signal.
- 1       9.     The transceiver of claim 1, further comprising command interpretation and  
2     command performance circuitry.
- 1       10.    The transceiver of claim 1, wherein the second and forth clock signals are  
2     synchronized.
- 1       11.    A system comprising:  
2              a first channel;  
3              a second channel;  
4              a first device coupled to the first channel;  
5              a second device coupled to the second channel; and  
6              a transceiver having latency aligning circuitry coupled to the first channel and  
7     to the second channel.
- 1       12.    The system of claim 11, wherein at least one of the first and second channels  
2     comprises a serial link.
- 1       13.    The system of claim 12, wherein data transmissions from the first device to the  
2     first channel are clocked by a first clock signal and wherein the latency aligning  
3     circuitry aligns the round-trip latency between the first device and the second channel  
4     to an integer number of cycles of the first clock signal.
- 1       14.    The system of claim 12, wherein the system has a round trip latency from the  
2     first device to the second device that is independent of a flight time from the first  
3     device to the second device.

- 1       15. The system of claim 14, wherein the latency aligning circuitry is configured to  
2 compensate for the flight time from the first device to the second device.
- 1       16. The system of claim 12, wherein a first latency, measured by a time required  
2 for the transceiver to receive a signal from the first channel and transmit the signal to  
3 the second channel, is dependent upon the flight time from the first device to the  
4 transceiver.
- 1       17. The system of claim 12, wherein the transceiver further comprises isolation  
2 logic to prevent retransmission of data, received from the first channel, to the second  
3 channel.
- 1       18. The system of claim 12, wherein the transceiver further comprises latch-up  
2 prevention logic to prevent feedback of data between the first and second channels.
- 1       19. The system of claim 12, wherein the transceiver further comprises a first  
2 synchronizing unit that synchronizes data transmitted from the first channel to the  
3 second channel.
- 1       20. The system of claim 19, wherein the transceiver further comprises a second  
2 synchronizing unit that synchronizes data transmitted from the second channel to the  
3 first channel.
- 1       21. The system of claim 12, wherein the transceiver further comprises power logic  
2 that turns off the transceiver when the transceiver does not need to transmit.
- 1       22. The system of claim 12, wherein data transmissions from the first device to the  
2 first channel are clocked by a first clock signal, data transmissions from the  
3 transceiver to the first channel are clocked by a second clock signal, data  
4 transmissions from the second device to the second channel are clocked by a third  
5 clock signal and data transmissions from the transceiver to the second device are  
6 clocked by a fourth clock signal.
- 1       23. The system of claim 22, wherein the second and fourth clock signals are  
2 synchronized.
- 1       24. The system of claim 12, wherein the transceiver further comprises at least one  
2 phase locked loop that performs clock recovery.
- 1       25. A memory system comprising  
2                  a memory controller coupled to a primary channel;

3           a first transceiver, having latency aligning circuitry, coupled to the primary  
4       channel and to a first stick channel.

5           a first memory device having a programmable delay coupled to the first stick  
6       channel; and

7           a second memory device having a programmable delay coupled to the primary  
8       channel or the first stick channel.

1       26. The memory system of claim 25, further comprising a second transceiver  
2       having latency aligning circuitry coupled to the stick channel and a second stick  
3       channel.

1       27. The memory system of claim 26, wherein the latency aligning circuitry of the  
2       first and second transceivers aligns a respective round-trip latency between the  
3       memory controller and each of the transceivers to a respective integer number of clock  
4       cycles.

1       28. The memory system of claim 27, wherein the round-trip latency between the  
2       memory controller and the first transceiver is a first integer number of clock cycles  
3       and the round-trip latency between the memory controller and the second transceiver  
4       is a second integer number of clock cycles and the first and second integer numbers  
5       are different.

1       29. The memory system of claim 26, further comprising a third memory device  
2       having programmable delay coupled to the second stick channel.

1       30. The memory system of claim 29, wherein the first memory device has a first  
2       programmed delay, the second memory device has a second programmed delay, the  
3       third memory device has a third programmed delay and wherein the first, second and  
4       third programmed delays are selected such that response latencies of the first, second  
5       and third memory devices are substantially equal.

1       31. The memory system of claim 25, wherein the first memory device has a first  
2       programmed delay and the second memory device has a second programmed delay  
3       and wherein the first and second programmed delays are selected such that response  
4       latencies of the first and second memory devices are substantially equal.

1       32. The memory system of claim 25, wherein the transceiver further comprises  
2       power logic to power off one or more of the transceivers when such transceivers do  
3       not need to transmit.